

## 受賞

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- Best Paper Award, The IEEE 13th International Symposium on Embedded Multicore/Many-core Systems-on-Chip (MCSoc), 2019.
- IEEE CEDA AJC Design Gaia Best Poster Award 2017, Design Gaia, 2017.
- Best Paper Award, The 3rd International Symposium on Computing and Networking (CANDAR'15), 2015.

## 研究費獲得歴

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- 特別研究員奨励費（DC2）1,900 (千円) 研究代表者

## 査読付き雑誌

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1. Francesco Conti, Gianna Paulin, Angelo Garofalo, Davide Rossi, Alfio Di Mauro, Georg Rutishauser, Gianmarco Ottavi, Manuel Eggiman, Hayate Okuhara, Luca Benini, "Marsellus: A Heterogeneous RIS C-V AI-IoT End-Node SoC With 2–8 b DNN Acceleration and 30%-Boost Adaptive Body Biasing," **IEEE Journal of Solid-State Circuits**, vol. 59, no. 1, pp. 128-142, Jan. 2024.
2. T. Kojima, H. Okuhara, M. Kondo and H. Amano, "A Scalable Body Bias Optimization Method Toward Low-Power CGRAs," **IEEE Micro**, vol. 43, no. 1, pp. 49-57, 1 Jan.-Feb. 2023.
3. H. Okuhara et al., "A Fully Integrated 5-mW, 0.8-Gbps Energy-Efficient Chip-to-Chip Data Link for Ultralow-Power IoT End-Nodes in 65-nm CMOS," **IEEE Transactions on Very Large Scale Integration (VLSI) Systems**, vol. 29, no. 10, pp. 1800-1811, Oct. 2021.
4. A. Elnaqib, H. Okuhara, T. Jang, D. Rossi and L. Benini, "A 0.5GHz 0.35mW LDO-Powered Constant-Slope Phase Interpolator With 0.22% INL," **IEEE Transactions on Circuits and Systems II: Express Briefs**, vol. 68, no. 1, pp. 156-160, Jan. 2021.
5. Hayate Okuhara, Akram Ben Ahmed, Hideharu Amano, "Digitally Assisted On-chip Body Bias Tuning Scheme for Ultra Low-power VLSI Systems," **IEEE Transactions on Circuits and Systems I: Regular Papers**, vol. 65, no. 10, pp. 3241-3254, Oct. 2018.
6. Hayate Okuhara, Akram Ben Ahmed, Johannes Maximilian Kühn, Hideharu Amano, "Asymmetric Body Bias Control with Low Power FD-SOI Technologies: Modeling and Power Optimization," **IEEE Transactions on Very Large Scale Integration Systems**, vol. 26, no. 7, pp. 1254-1267, July 2018.
7. Koichiro Masuyama, Yu Fujita, Hayate Okuhara, Hideharu Amano, "Ultra Low Power Reconfigurable Accelerator," **IEICE Transactions on Information and Systems**, vol. J101-D, no. 5, pp.729-741, May 2018. (in Japanese)
8. Carlos Cesar Cortes Torres, Hayate Okuhara, Nobuyuki Yamasaki, Hideharu Amano, "Analysis of Body Bias Control Using Overhead Conditions for Real Time Systems: A Practical Approach," **IEICE T**

ransactions on Information and Systems, vol. E101-D, no. 4, pp.1116-1125, April 2018.

9. Yusuke, Matsushita, Hayate Okuhara, Koichiro Masuyama, Yu Fujita, Ryuta Kawano, Hideharu Amano, "Body Bias Domain Partitioning Size Exploration for Coarse Grained Reconfigurable Accelerator," IEICE Transactions on Information and Systems, vol. E100-D, no. 12, pp.2828-2836, Dec. 2017.
10. H. Okuhara, Y. Fujita, K. Usami and H. Amano, "Power Optimization Methodology for Ultralow Power Microcontroller With Silicon on Thin BOX MOSFET," **IEEE Transactions on Very Large Scale Integration (VLSI) Systems**, vol. 25, no. 4, pp. 1578-1582, April 2017.
11. Hayate Okuhara, Kuniaki Kitamori, Kimiyoshi Usami, Hideharu Amano, "A Research of Dynamic Body Bias Control on Micro Controller V850 Using SOTB MOSFET," The IPSJ Journal, vol. 57, no. 2, pp.708-717, Feb. 2016. (in Japanese)

## 国際会議

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1. H. Okuhara, U. D. Alwis, L. Yue, K. A. Ahmed and M. Alioto, "Smart Imager with Object Detection Exploiting Edge-Frame-Base Processing and Bounding Box Extraction for  $\mu$ W Power Purely-Harvested Sensor Nodes," **2026 Design, Automation & Test in Europe Conference (DATE)**, Verona, Italy, 2026, pp. 1-7.
2. T. Kojima, Y. Yanai, H. Okuhara, H. Amano, M. Kuga and M. Iida, "SLMLET: A RISC-V Processor SoC with Tightly-Coupled Area-Efficient eFPGA Blocks," 2024 IEEE Symposium on Low-Power and High-Speed Chips (COOL CHIPS), Tokyo, Japan, 2024, pp. 1-6
3. K. A. Ahmed\*, H. Okuhara\*, M. Alioto, "55-pW/pixel Peak Power Imager with Near-Sensor Novelty /Edge Detection and DC-DC Converter-Less MPPT for Purely-Harvested Sensor Nodes," **2023 IEEE International Solid-State Circuits Conference (ISSCC)**, San Francisco, CA, USA, 2023, pp. 102-104. (\* **Equally Contributed Authors:共同筆頭**)
4. Francesco Conti, Davide Rossi, Gianna Paulin, Angelo Garofalo, Alfio Di Mauro, Georg Rutishauer, Gian marco Ottavi, Manuel Eggimann, Hayate Okuhara, Vincent Huard, Olivier Montfort, Lionel Jure, Nils Exibard, Pascal Gouedo, Mathieu Louvat, Emmanuel Botte, Luca Benini., "22.1 A 12.4TOPS/W @ 136GOPS AI-IoT System-on-Chip with 16 RISC-V, 2-to-8b Precision-Scalable DNN Acceleration and 30%-Boost Adaptive Body Biasing," **2023 IEEE International Solid-State Circuits Conference (ISSCC)**, San Francisco, CA, USA, 2023, pp. 21-23.
5. Hayate Okuhara, Ahmed Elnaqib, Davide Rossi, Alfio Di Mauro, Philipp Mayer, Pierpaolo Palestri, Luca Benini, "An Energy-Efficient Low-Voltage Swing Transceiver for mW-Range IoT End-Nodes", 2020 IEEE International Symposium on Circuits and Systems (ISCAS), Seville, Spain, 2020, pp. 1-5.
6. H. Kayashima, T. Kojima, H. Okuhara, T. Shidei and H. Amano, "Real Chip Performance Evaluation on Through Chip Interface IP for Renesas SOTB 65nm Process," 2019 Seventh International Symposium on Computing and Networking Workshops (CANDARW), Nagasaki, Japan, 2019, pp. 269-274.

7. Hayate Okuhara, Ryosuke Kazami, Hideharu Amano, "A System Delay Monitor Exploiting Automatic Cell-Based Design Flow and Post-Silicon Calibration," 2019 IEEE 13th International Symposium on Embedded Multicore/Many-core Systems-on-Chip (MCSoc), Singapore, 2019, pp. 32-37.
8. Sayaka Terashima, Takuya Kojima, Hayate Okuhara, Kazusa Musha, Hideharu Amano, Ryuichi Sakamoto, Masaaki Kondo, Mitaro Namiki, "A Preliminary Evaluation of Building Block Computing Systems," 2019 IEEE 13th International Symposium on Embedded Multicore/Many-core Systems-on-Chip (MCSoc), Singapore, 2019, pp. 312-319.
9. A. Ben Ahmed, H. Okuhara, H. Matsutani, M. Koibuchi and H. Amano, "Adaptive Body Bias Control Scheme for Ultra Low-Power Network-on-Chip Systems," 2018 IEEE 12th International Symposium on Embedded Multicore/Many-core Systems-on-Chip (MCSoc), Hanoi, Vietnam, 2018, pp. 146-153.
10. R. Kazami, H. Okuhara and H. Amano, "Design automation methodology of a critical path monitor for adaptive voltage controls," 2018 IEEE Symposium on Low-Power and High-Speed Chips (COOL CHIPS), Yokohama, Japan, 2018, pp. 1-3.
11. Sayaka Terashima, Takuya Kojima, Hayate Okuhara, Yusuke Matsushita, Naoki Ando, Mitaro Namiki, Hideharu Amano, "A Shared Memory Chip for Twin-Tower of Chips," 21st Workshop on Synthesis And System Integration of Mixed Information Technologies (SASIMI2018), Matsune, Japan, 2018, pp. 353-358.
12. Takuya Kojima, Naoki Ando, Hayate Okuhara, Hideharu Amano, "Glitch-aware variable pipeline optimization for CGRAs," 2017 International Conference on ReConFigurable Computing and FPGAs (ReConFig), Cancun, Mexico, 2017, pp. 1-6.
13. T. Kojima, N. Ando, H. Okuhara, N. A. Vu Doan and H. Amano, "Body bias optimization for variable pipelined CGRA," 2017 27th International Conference on Field Programmable Logic and Applications (FPL), Ghent, Belgium, 2017, pp. 1-4.
14. H. Okuhara, A. Ben Ahmed, J. M. Kühn and H. Amano, "Leveraging asymmetric body bias control for low power LSI design," 2017 IEEE Symposium in Low-Power and High-Speed Chips (COOL CHIPS), Yokohama, Japan, 2017, pp. 1-3.
15. Naoki Ando, Koichiro Masuyama, Hayate Okuhara, Hideharu Amano, "Variable pipeline structure for Coarse Grained Reconfigurable Array CMA," 2016 International Conference on Field-Programmable Technology (FPT), Xi'an, China, 2016, pp. 217-220.
16. Yusuke Matsushita, Hayate Okuhara, Koichiro Masuyama, Yu Fujita, Ryuta Kawano, Hideharu Amano, "Body bias grain size exploration for a coarse grained reconfigurable accelerator," 2016 26th International Conference on Field Programmable Logic and Applications (FPL), Lausanne, Switzerland, 2016, pp. 1-4.
17. J. M. Kühn, A. Ben Ahmed, H. Okuhara, H. Amano, O. Bringmann and W. Rosenstiel, "MuCCRA4-BB: A fine-grained body biasing capable DRP," 2016 IEEE Symposium in Low-Power and High-Speed

ed Chips (COOL CHIPS XIX), Yokohama, Japan, 2016, pp. 1-3.

18. K. Masuyama, Y. Fujita, H. Okuhara and H. Amano, "A 297mops/0.4mw ultra low power coarse-grained reconfigurable accelerator CMA-SOTB-2," 2015 International Conference on ReConFigurable Computing and FPGAs (ReConFig), Riviera Maya, Mexico, 2015, pp. 1-6.
19. Yu Fujita, Hayate Okuhara, Koichiro Masuyama, Hideharu Amano, "Power Optimization Considering the Chip Temperature of Low Power Reconfigurable Accelerator CMA-SOTB," 2015 Third International Symposium on Computing and Networking (CANDAR), Sapporo, Japan, 2015, pp. 21-29.
20. H. Okuhara, K. Kitamori, Y. Fujita, K. Usami and H. Amano, "An optimal power supply and body bias voltage for a ultra low power micro-controller with silicon on thin box MOSFET," **2015 IEEE/ACM International Symposium on Low Power Electronics and Design (ISLPED)**, Rome, Italy, 2015, pp. 207-212.
21. H. Okuhara, K. Usami and H. Amano, "A leakage current monitor circuit using silicon on thin BOX MOSFET for dynamic back gate bias control," 2015 IEEE Symposium in Low-Power and High-Speed Chips (COOL CHIPS XVIII), Yokohama, Japan, 2015, pp. 1-3.
22. Hayate Okuhara, Hideharu Amano, "Time Analysis of Applying Back Gate Bias for Reconfigurable Architectures with SOTB MOSFET", 19th Workshop on Synthesis and System Integration of Mixed Information Technologies (SASIMI2015), Yilan, Taiwan, 2015, pp.299-304.